CLAIMS

What is claimed is:

1. A serially-programmable integrated circuit (IC) comprising:

a first input connector for receiving serial programming data;

a memory array having a first width, the memory array comprising a plurality of primary columns and a plurality of redundant columns, the plurality of primary columns having a second width and the plurality of redundant columns having a third width;

a data register coupled to receive the serial programming data from the first input connector, the data register comprising a shift register having a fourth width, the fourth width being a divisor of the second width and the third width;

a bitline latch for loading a data word into the memory array, the bitline latch having the first width; and

a column multiplexer for performing a loading operation to load data in parallel from the data register into the bitline latch.

2. The serially-programmable IC of Claim 1, wherein the memory array is organized into a plurality of column groupings, each of the column groupings having the fourth width, and wherein the bitline latch is organized into a plurality of latch groupings, each of the latch groupings having the fourth width, each of the plurality of latch groupings being associated with one of the plurality of column groupings.

3. The serially-programmable IC of Claim 2, further comprising a shift control circuit for providing an address signal to the column multiplexer, the address signal instructing the column multiplexer to load data from the data register into a selected one of the plurality of latch groupings.

4. The serially-programmable IC of Claim 3, wherein the shift control circuit comprises:

a counter circuit for generating a count value, wherein the shift control circuit increments the counter circuit each time the column multiplexer performs the loading operation; and

an address decoder for generating the address signal from the count value.

5. The serially-programmable IC of Claim 4, wherein the plurality of latch groupings includes a plurality of primary latch groupings associated with the plurality of primary columns and a redundant latch grouping associated with the plurality of redundant columns, wherein the shift control circuit further comprises a redundancy circuit for comparing the count value to a predetermined count value, the predetermined count value corresponding to a first one of the plurality of primary latch groupings, the first one of the plurality of latch groupings being associated with a first one of the plurality of column groupings, the first one of the plurality of column groupings including a memory defect, wherein when the count value matches the predetermined count value, the redundancy circuit asserts a redundancy enable signal instructing the column multiplexer to load data from the data register into the redundant latch grouping.

6. The serially-programmable IC of Claim 5, wherein the redundancy circuit comprises a content addressable memory (CAM) for storing the predetermined count value.

7. The serially-programmable IC of Claim 5, wherein when the plurality of redundant columns are in use, the redundancy circuit asserts a redundant-column-on signal, the redundant-column-on signal enabling the redundancy enable signal.

8. The serially-programmable IC of Claim 7, wherein the address signal comprises a plurality of word indicator bits and a plurality of column indicator bits, and wherein the address decoder comprises:

a word decoder for decoding a first portion of the count value into the plurality of word indicator bits; and

a column decoder for decoding a second portion of the count value into the plurality of column indicator bits.

9. The serially-programmable IC of Claim 8, wherein the data register comprises a plurality of flip flops, wherein each of the plurality of latch groupings comprises a plurality of latches, and wherein the column multiplexer comprises:

a first plurality of pass transistor groupings, each of the first plurality of pass transistor groupings comprising a plurality of pass transistor sets, each of the pass transistor sets being coupled between one of the plurality of flip flops and one of the plurality of latches in one of the plurality of primary latch groupings, each of the plurality of pass transistor sets in each of the first plurality of pass

transistor groupings comprising a first transistor and a second transistor coupled in series, with the gate of the first pass transistor being coupled to receive one of the plurality of column indicator bits and the gate of the second pass transistor being coupled to receive one of the plurality of word indicator bits; and

a redundant pass transistor grouping comprising a plurality of individual pass transistors, each of the individual pass transistors being coupled between one of the plurality of flip flops and one of the plurality of latches in the redundant latch grouping, the gates of each of the individual pass transistors being coupled to receive the redundancy enable signal.

10. The serially-programmable IC of Claim 4, wherein the serially-programmable IC comprises a Joint Test Action Group (JTAG) programmable IC, and wherein the first input connector comprises a test data input (TDI) terminal.

11. The serially-programmable IC of Claim 10, further comprising:

an instruction register coupled to receive an instruction bitstream via the TDI terminal;

an instruction decoder for decoding the instruction bitstream stored in the instruction register to generate an instruction signal; and

a test access port (TAP) controller for providing JTAG states in response to a test mode select (TMS) signal and a test clock (TCK) signal,

wherein the shift control circuit further comprises a counter controller coupled to the TAP controller, wherein when the instruction signal is equal to a specified data loading instruction, the counter circuit generates a counter

enable signal in response to a JTAG SHIFT-DR state from the TAP controller, the counter enable signal incrementing the counter circuit.

12. The serially-programmable IC of Claim 1, wherein the serially-programmable IC comprises an electrically erasable programmable read only memory (EEPROM).

13. The serially-programmable IC of Claim 1, wherein the serially-programmable IC comprises a FLASH memory.

14. A method for programming a memory array on an integrated circuit (IC), the method comprising:

setting the counter value in a counter circuit on the IC equal to an initial counter value;

shifting a portion of a serial programming bitstream into a partial-width data register on the IC, wherein a width of the partial-width data register is less than a width of the memory array;

comparing the counter value to a predetermined defect value, the predetermined defect value being associated with a defective column grouping in the memory array;

loading the portion of the serial programming bitstream into a primary latch grouping on the IC if the counter value does not match the predetermined defect value, wherein the primary latch grouping is associated with a primary column grouping in the memory array; and

loading the portion of the serial programming bitstream into a redundant latch grouping on the IC if the counter value matches the predetermined defect value, wherein the redundant latch grouping is

associated with a redundant column grouping in the memory array.

15. The method of Claim 14, wherein the IC further comprises a test data input (TDI) terminal, a test mode select (TMS) terminal for receiving a TMS signal, a test clock (TCK) terminal for receiving a clock signal, and a test access port (TAP) controller coupled to the TMS terminal and the TCK terminal, the TAP controller being controlled by the TMS signal and the TCK signal, and wherein shifting the portion of the serial programming bitstream into the partial-width data register comprises:

placing the TAP controller in a Joint Test Action Group (JTAG) SHIFT-DR state; and

shifting a bit from the serial programming bitstream through the TDI terminal into the partial-width data register at each pulse of the clock signal; and

placing the TAP controller in a JTAG EXIT1-DR state once the data register is filled with bitstream data from the programming bitstream.

16. The method of Claim 15, wherein loading the portion of the serial programming bitstream into the primary latch grouping comprises:

generating a bitline position indicator from the counter value when the counter value does not match the predetermined defect value, the bitline position indicator being associated with the primary latch grouping;

placing the TAP controller in a JTAG UPDATE-DR state;

loading data from the partial-width data register in parallel into the primary latch grouping; and

placing the TAP controller in a JTAG RUN-TEST-IDLE state.

17. The method of Claim 16, wherein generating the bitline position indicator comprises:

generating a plurality of word indicator signals from a first portion of the counter value; and

generating a plurality of column indicator signals from a second portion of the counter value.

18. The method of Claim 16, wherein loading the portion of the serial programming bitstream into the redundant latch grouping comprises:

generating a redundancy enable signal when the counter value matches the predetermined defect value;

placing the TAP controller in the JTAG UPDATE-DR state;

loading data from the partial-width data register in parallel into the redundant latch grouping in response to the redundancy enable signal; and

placing the TAP controller in the JTAG RUN-TEST-IDLE state.

19. The method of Claim 18, wherein incrementing the counter value in the counter circuit comprises placing the TAP controller in a JTAG SELECT-DR state.

20. An integrated circuit (IC) comprising:

a Test Access Port (TAP) port including a test data input (TDI) terminal;

a memory array having a first width, the memory array including a plurality of primary columns and a plurality of redundant columns;

a data register coupled to the TDI terminal, the data register having a second width, the second width being less than the first width; and

a bitline latch coupled between the data register and the memory array, the bitline latch having the first width.

21. The IC of Claim 20, further comprising means for loading a programming bitstream into the bitline latch by shifting successive portions of the programming bitstream into the data register and then loading each of the successive portions of the programming bitstream from the data register into the bitline latch.

22. The IC of Claim 21, wherein the memory array is organized into a plurality of primary column groupings and at least one redundant column grouping, each of the plurality of primary column groupings having a primary column grouping width equal to the second width, and the at least one redundant column grouping having a redundant column grouping width equal to the second width, wherein the IC further comprises means for assigning a position indicator to each of the successive portions of the programming bitstream, each position indicator being associated with one of the plurality of primary column groupings.

23. The IC of Claim 22, wherein the means for assigning the position indicator comprises a counter circuit for incrementing a counter value for each of the successive

portions of the programming bitstream shifted into the data register, the counter value providing the position indicator.

24. The IC of Claim 23, wherein the bitline latch is organized into a plurality of latch groupings, each of the plurality of latch groupings having a latch grouping width equal to the second width and each of the plurality of latch groupings being associated with one of the plurality of primary column groupings or the at least one redundant column grouping, the IC further comprising

means for comparing the position indicator for the portion of the programming bitstream in the data register with a defective column position indicator;

means for loading the portion of the programming bitstream in the data register into the latch grouping associated with the primary column grouping associated with the position indicator assigned to the programming bitstream in the data register when the position indicator assigned to the portion of the programming bitstream in the data register does not match the defective column position indicator; and

means for loading the portion of the programming bitstream in the data register into the at least one redundant column grouping when the position indicator assigned to the portion of the programming bitstream in the data register matches the defective column position indicator.

25. The IC of Claim 24, wherein the means for comparing the position indicator comprises a content addressable memory (CAM) for storing the defective column position indicator.

26. The IC of Claim 25, wherein the CAM asserts a match signal when the position indicator assigned to the portion of the programming bitstream in the data register matches the defective column position indicator, and wherein the means for loading the portion of the programming bitstream in the data register into the at least one redundant column grouping comprises a column multiplexer, the column multiplexer loading the portion of the programming bitstream in the data register into the latch grouping associated with the at least one redundant column grouping in response to the match signal.

27. The IC of Claim 26, wherein the means for loading the portion of the programming bitstream in the data register into the latch grouping associated with the primary column grouping associated with the position indicator comprises an address decoder for decoding the position indicator into a local address when the match signal is not asserted, the local address instructing the column multiplexer to load the portion of the programming bitstream in the data register into the latch grouping associated with the primary column grouping associated with the position indicator.